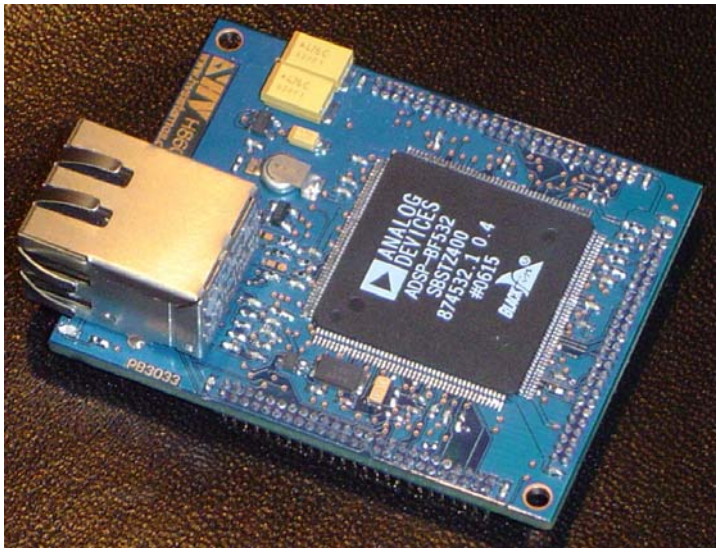
HV Sistemas S.L.

H8606

BLACKFIN EMBEDDED PROCESSOR BOARD



FEATURES

- 400 MHz Analog Devices ADSP-BF532 Blackfin Digital Signal Processor
- 3.3V single supply
- U-Boot bootloader
- uClinux ready
- 32Mb 133MHz SDRAM memory
- 8Mb (16Mb as option) Serial FLASH memory
- 100Mb integral Ethernet interface
- All ADSP-BF532 DSP integrated peripherals and bus signals are accessible at the board connectors
- 100,000-gate (250,000-gate as option) Xilinx Spartan 3E FPGA for maximum peripheral flexibility
- Integral rechargeable lithium battery for real-time clock

APPLICATIONS

- General purpose processor for industrial applications
- Telecommunications
- Audio and video signal processing
- Prototyping, small and medium volume applications

DESCRIPTION

HV Sistemas H8606 is a low-cost embedded processor board with a small form-factor and low power requisites, yet providing high processing power and flexibility.

It is built around an Analog Devices ADSP-BF532 Digital Signal Processor, and has being designed to run uClinux as operating system, including Adeos/Xenomai Real Time Extensions.

Due to its small size and low power requirements, this board can be easily integrated into products, enabling the designer great flexibility and a reduced time to market.

This board provides accessibility to most of the ADSP-BF532 bus and peripheral pins, so all the ADSP-BF532 integrated peripherals are available to the user. Additionally, incorporates a 10/100Mbps Ethernet controller with standard RJ-45 connector incorporating magnetics, plus a 100,000-gate (250,000-gate as option) Xilinx Spartan 3E FPGA that enables to add additional peripheral functions, as for example UARTS, I2C controllers, etc.

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ARCHITECTURE

HV Sistemas H8606 uses as CPU an Analog Devices ADSP-BF532 digital signal processor, running at a maximum core frequency of 400MHz and a maximum peripheral frequency of 133MHz. This processor is fully supported in the Blackfin-uClinux distribution, including drivers for all its integrated peripherals, as well as a variety of peripheral emulations (for example, I2C emulation using PF pins or UART emulation using SPORTs). Processor clock is generated from a 25MHz quartz crystal, and a buffered 25MHz output is provided.

The integrated ADSP-BF532 real time clock uses a 32768Hz quartz crystal, and is supplied by an on-board rechargeable lithium battery.

The board is powered from a 3.3V single supply, and includes all the necessary on-board regulators for generating 1.2V processor core and FPGA core, as well as 2.5V FPGA power supplies.

This board incorporates also a 8Mb M25P64 (16Mb S25FL128 as option) serial FLASH memory, where the U-Boot, FPGA and uClinux code resides, leaving more than 6Mb (or 14Mb) free for use as solid-state disk, than can use a JFFS2 filesystem.

RAM memory is 32Mb SDRAM type, running at 133MHz.

Additionaly to the ADSP-BF532 peripherals, the board includes a DM9000A-based 10/100Mbps Ethernet controller, supported both by U-Boot and uClinux.

The board incorporates a Xilinx XC3S100E-4VQG100 FPGA, in 100-pin VQFP package (XC3S250E-4VQG100 as option). This FPGA incorporates 100,000 gates (or 250,000 gates), and is connected to the ADSP-BF352, getting data bus D0–D7 signals, address bus A1-A5 signals, and all the bus control signals, enabling the user to add additional peripheral functions in the FPGA. If other data bus or address bus signals are needed for the FPGA, they can be routed externally from the desired ADSP-BF532 pin to any of the available FPGA pins. FPGA code resides in the FLASH memory, and is easily loaded in the FPGA by the U-boot loader. The user can easily upload FPGA code in the FLASH memory through U-boot using serial interface or Ethernet interface.

DEVELOPMENT KIT

HV Sistemas H8606-DK is a low-cost development kit that includes small board that incorporating 5V and 3.3V voltage regulators, RS-232 interface and DB9 connector for UART0, buffered processor address, data and bus control signals, and provides easy access to al H8606 signals through standard 0.100” (2.54mm) headers, for easy evaluation of the processor board and prototyping. It is supplied along with the uClinux distribution, including specific support to H8606 board, and the Blackfin gcc compiler.

ELECTRICAL SPECIFICATIONS

Power supply voltage range	3.3Vcc +/-5%
Power supply current	500mA máx
I/O levels	3.3V LVTTL – Please consult relevant ADSP-BF532 and XC3S100 data sheets for detailed specifications
Crystal oscillator frequency	25.000 MHz
Connectors	3 x 50-way 0.050” (1.27mm) pitch dual row connectors for power supply and interface RJ-45 integral connector for Ethernet interface

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PIN CONFIGURATION AND FUNCTION DESCRIPTION

CONNECTOR J1

Pin #	Signal Name	Function	Pin #	Signal Name	Function
J1-1	Vcc	+3.3V power supply input	J1-26	A14	ADSP-BF532 A14 (Address bus)(1)
J1-2	GND	Power supply ground	J1-27	A13	ADSP-BF532 A13 (Address bus)(1)
J1-3	D15	ADSP-BF532 D15 (Data bus)(1)	J1-28	A12	ADSP-BF532 A12 (Address bus)(1)
J1-4	D14	ADSP-BF532 D14 (Data bus)(1)	J1-29	A11	ADSP-BF532 A11 (Address bus)(1)
J1-5	D13	ADSP-BF532 D13 (Data bus)(1)	J1-30	A10	ADSP-BF532 A10 (Address bus)(1)
J1-6	D12	ADSP-BF532 D12 (Data bus)(1)	J1-31	A9	ADSP-BF532 A9 (Address bus)(1)
J1-7	D11	ADSP-BF532 D11 (Data bus)(1)	J1-32	A8	ADSP-BF532 A8 (Address bus)(1)
J1-8	D10	ADSP-BF532 D10 (Data bus)(1)	J1-33	A7	ADSP-BF532 A7 (Address bus)(1)
J1-9	D9	ADSP-BF532 D9 (Data bus)(1)	J1-34	A6	ADSP-BF532 A6 (Address bus)(1)
J1-10	D8	ADSP-BF532 D8 (Data bus)(1)	J1-35	A5	ADSP-BF532 A5 (Address bus)(1)
J1-11	D7	ADSP-BF532 D7 (Data bus)(1)	J1-36	A4	ADSP-BF532 A4 (Address bus)(1)
J1-12	D6	ADSP-BF532 D6 (Data bus)(1)	J1-37	A3	ADSP-BF532 A3 (Address bus)(1)
J1-13	D5	ADSP-BF532 D5 (Data bus)(1)	J1-38	A2	ADSP-BF532 A2 (Address bus)(1)
J1-14	D4	ADSP-BF532 D4 (Data bus)(1)	J1-39	A1	ADSP-BF532 A1 (Address bus)(1)
J1-15	D3	ADSP-BF532 D3 (Data bus)(1)	J1-40	ARDY	ADSP-BF532 ARDY(1)
J1-16	D2	ADSP-BF532 D2 (Data bus)(1)	J1-41	AMS3-	ADSP-BF532 AMS3-(1)
J1-17	D1	ADSP-BF532 D1 (Data bus)(1)	J1-42	AMS2-	ADSP-BF532 AMS2-(1)
J1-18	D0	ADSP-BF532 D0 (Data bus)(1)	J1-43	AMS1-	ADSP-BF532 AMS1-(1)(3)
J1-19	BG-	ADSP-BF532 BG-(1)	J1-44	AMS0-	ADSP-BF532 AMS0-(1)
J1-20	BGH-	ADSP-BF532 BGH-(1)	J1-45	ARE-	ADSP-BF532 ARE-(1)
J1-21	A19	ADSP-BF532 A19 (Address bus)(1)	J1-46	AOE-	ADSP-BF532 AOE-(1)
J1-22	A18	ADSP-BF532 A18 (Address bus)(1)	J1-47	AWE-	ADSP-BF532 AWE-(1)
J1-23	A17	ADSP-BF532 A17 (Address bus)(1)	J1-48	CLK_25MHz	25MHz buffered output from ADSP-BF532 cristal osillator
J1-24	A16	ADSP-BF532 A16 (Address bus)(1)	J1-49	Vcc	+3.3V power supply input
J1-25	A15	ADSP-BF532 A15 (Address bus)(1)	J1-50	GND	Power supply ground

Notes:

(1) These pins are direct connections to the corresponding ADSP-BF532 pins

(2) These pins are direct connections to the corresponding XC3S100E-4VQG100 (XC3S250E-4VQG100 as option) FPGA pins, and can be freely used as inputs or outputs

(3) AMS1- is also used for Ethernet controller chip select

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PIN CONFIGURATION AND FUNCTION DESCRIPTION (continued)

CONNECTOR J2

Pin #	Signal Name	Function	Pin #	Signal Name	Function
J2-1	Vcc	+3.3V power supply input	J2-26	BMODE1	ADSP-BF532 BMODE1(1)(3)
J2-2	GND	Power supply ground	J2-27	FPGA57	FPGA pin 57 (input/output) (2)
J2-3	TMR1	ADSP-BF532 TMR1(1)	J2-28	FPGA58	FPGA pin 58 (input/output) (2)
J2-4	TMR2	ADSP-BF532 TMR2(1)	J2-29	FPGA60	FPGA pin 60 (input/output) (2)
J2-5	PPICLK	ADSP-BF532 PPICLK(1)	J2-30	FPGA61	FPGA pin 61 (input/output) (2)
J2-6	PF3	ADSP-BF532 PF3(1)	J2-31	FPGA62	FPGA pin 62 (input/output) (2)
J2-7	PF4	ADSP-BF532 PF4(1)	J2-32	FPGA63	FPGA pin 63 (input/output) (2)
J2-8	PF5	ADSP-BF532 PF5(1)	J2-33	FPGA65	FPGA pin 65 (input/output) (2)
J2-9	PF6	ADSP-BF532 PF6(1)	J2-34	FPGA66	FPGA pin 66 (input/output) (2)
J2-10	PF7	ADSP-BF532 PF7(1)	J2-35	FPGA67	FPGA pin 67 (input/output) (2)
J2-11	PF8	ADSP-BF532 PF8 and FPGA pin 44(1)(6)	J2-36	FPGA68	FPGA pin 68 (input/output) (2)
J2-12	PF9	ADSP-BF532 PF9 and FPGA pin 50(1)(6)	J2-37	FPGA70	FPGA pin 70 (input/output) (2)
J2-13	PF10	ADSP-BF532 PF10(1)(5)	J2-38	FPGA71	FPGA pin 71 (input/output) (2)
J2-14	PF11	ADSP-BF532 PF11(1)	J2-39	FPGA78	FPGA pin 78 (input/output) (2)
J2-15	PF12	ADSP-BF532 PF12(1)	J2-40	FPGA79	FPGA pin 79 (input/output) (2)
J2-16	PF13	ADSP-BF532 PF13(1)	J2-41	FPGA25	FPGA pin 25 (input/output) (2)
J2-17	PF14	ADSP-BF532 PF14(1)	J2-42	FPGA84	FPGA pin 84 (input/output) (2)
J2-18	PF15	ADSP-BF532 PF15(1)	J2-43	FPGA85	FPGA pin 85 (input/output) (2)
J2-19	PPI3	ADSP-BF532 PPI3(1)	J2-44	FPGA86	FPGA pin 86 (input/output) (2)
J2-20	PPI2	ADSP-BF532 PPI2(1)	J2-45	FPGA88	FPGA pin 88 (input/output) (2)
J2-21	PPI1	ADSP-BF532 PPI1(1)	J2-46	RST_IN-	Reset input(4)
J2-22	PPI0	ADSP-BF532 PPI0(1)	J2-47	FPGA90	FPGA pin 90 (input/output) (2)
J2-23	NMI	ADSP-BF532 NMI(1)	J2-48	FPGA91	FPGA pin 91 (input/output) (2)
J2-24	BR-	ADSP-BF532 BR-(1)	J2-49	Vcc	+3.3V power supply input
J2-25	BMODE0	ADSP-BF532 BMODE0(1)(3)	J2-50	GND	Power supply ground

Notes:

(1) These pins are direct connections to the corresponding ADSP-BF532 pins

(2) These pins are direct connections to the corresponding XC3S100E-4VQG100 (XC3S250E-VQG100 as option) FPGA pins, and can be freely used as inputs or outputs

(3) Board includes pull-up resistors in these inputs, so they can be left unconnected for SPI Flash booting

(4) Can be left unconnected

(5) Shared with Ethernet controller interrupt – Ethernet controller interrupt can optionally routed through the FPGA

(6) These pins are also used during boot for FPGA loading, and its levels must not be disturbed during boot. After booting they can be used as inputs or outputs.

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PIN CONFIGURATION AND FUNCTION DESCRIPTION (continued)

CONNECTOR J3

Pin #	Signal Name	Function	Pin #	Signal Name	Function
J3-1	Vcc	+3.3V power supply input	J3-26	TFS1	ADSP-BF532 SPORT1 TFS(1)
J3-2	GND	Power supply ground	J3-27	DT1PRI	ADSP-BF532 SPORT1 DTPRI(1)
J3-3	TDO	ADSP-BF532 JTAG TDO(1)	J3-28	DT1SEC	ADSP-BF532 SPORT1 DTSEC(1)
J3-4	TDI	ADSP-BF532 JTAG TDI(1)	J3-29	SPI_MOSI	ADSP-BF532 SPI MOSI (Master Output – Slave Input) (1)
J3-5	TMS	ADSP-BF532 JTAG TMS(1)	J3-30	SPI_MISO	ADSP-BF532 SPI MISO (Master Input – Slave Output) (1)
J3-6	TRST-	ADSP-BF532 JTAG TRST-(1)	J3-31	SPI_CLK	ADSP-BF532 SPI clock(1)
J3-7	EMU-	ADSP-BF532 JTAG EMU-(1)	J3-32	PF0/SPISS-	ADSP-BF532 PF0(1)
J3-8	TCK	ADSP-BF532 JTAG TCK(1)	J3-33	PF1/SPISEL1/ TMRCLK	ADSP-BF532 PF1(1)
J3-9	RXD0	ADSP-BF532 UART RXD(1)	J3-34	PF2/SPISEL2	ADSP-BF532 PF2(1)(4)
J3-10	TXD0	ADSP-BF532 UART TXD(1)	J3-35	FPGA32	FPGA pin 32 (input/output) (2)
J3-11	TMR0	ADSP-BF532 Timer 0(1)	J3-36	FPGA33	FPGA pin 33 (input/output) (2)
J3-12	FPGA69	FPGA pin 69 (input only) (2)	J3-37	FPGA34	FPGA pin 34 (input/output) (2)
J3-13	RSCLK0	ADSP-BF532 SPORT0 RSCLK(1)	J3-38	FPGA35	FPGA pin 35 (input/output) (2)
J3-14	RFS0	ADSP-BF532 SPORT0 RFS(1)	J3-39	FPGA36	FPGA pin 36 (input/output) (2)
J3-15	DR0PRI	ADSP-BF532 SPORT0 DRPRI(1)	J3-40	FPGA40	FPGA pin 40 (input/output) (2)
J3-16	DR0SEC	ADSP-BF532 SPORT0 DRSEC(1)	J3-41	FPGA41	FPGA pin 41 (input/output) (2)
J3-17	TSCLK0	ADSP-BF532 SPORT0 TSCLK(1)	J3-42	FPGA42	FPGA pin 42 (input/output) (2)(3)
J3-18	TFS0	ADSP-BF532 SPORT0 TFS(1)	J3-43	FPGA43	FPGA pin 43 (input/output) (2)(3)
J3-19	DT0PRI	ADSP-BF532 SPORT0 DTPRI(1)	J3-44	FPGA47	FPGA pin 47 (input/output) (2)
J3-20	DT0SEC	ADSP-BF532 SPORT0 DTSEC(1)	J3-45	FPGA48	FPGA pin 32 (input/output) (2)
J3-21	RSCLK1	ADSP-BF532 SPORT1 RSCLK(1)	J3-46	FPGA49	FPGA pin 33 (input/output) (2)
J3-22	RFS1	ADSP-BF532 SPORT1 RFS(1)	J3-47	FPGA53	FPGA pin 34 (input/output) (2)
J3-23	DR1PRI	ADSP-BF532 SPORT1 DRPRI(1)	J3-48	FPGA54	FPGA pin 35 (input/output) (2)
J3-24	DR1SEC	ADSP-BF532 SPORT1 DRSEC(1)	J3-49	Vcc	+3.3V power supply input
J3-25	TSCLK1	ADSP-BF532 SPORT1 TSCLK(1)	J3-50	GND	Power supply ground

Notes:

(1) These pins are direct connections to the corresponding ADSP-BF532 pins

(2) These pins are direct connections to the corresponding XC3S100E-4VQG100 (XC3S100E-4VQG100 as option) FPGA pins, and can be freely used as inputs or outputs

(3) These pinst must be at a high logic level during reset, since they also sets the FPGA boot mode

(4) PF2 is used for internal serial FLASH memory chip select

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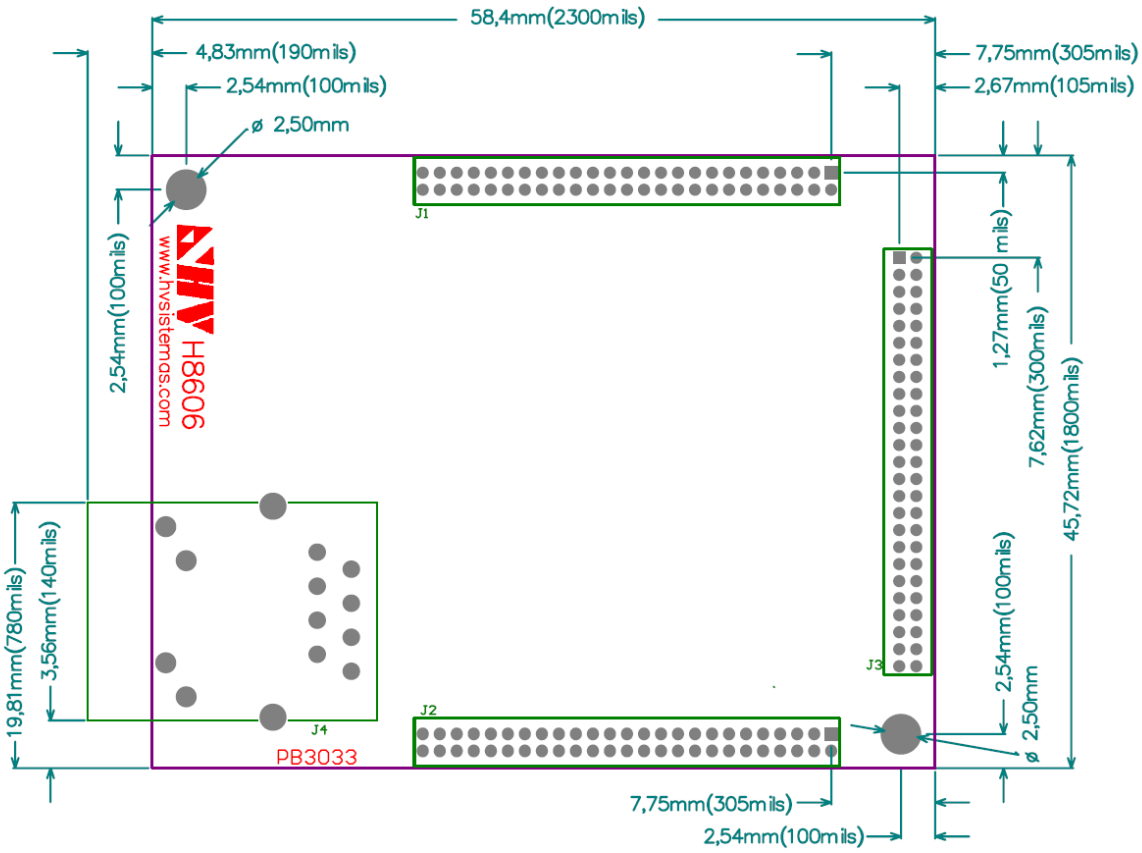
BOARD DIMENSIONS AND CONNECTOR LOCATION



(Top view)

Mating connectors for J1, J2, J3: 2x25 ways 1.27mm (0.050") dual row headers, SAMTEC CLP and FLE series or Harwin M50-3102545, among others

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